Wideband Data on T1 Carrier

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The T1 carrier repeatered line is the Bell System's first high-speed digital transmission facility. Although developed primarily for the transmission of analog information in the form of processed voice frequency signals, its potential use as a short-haul data facility has stimulated considerable interest and study. T1 carrier data terminal designs are described for various general types of applications, and consideration is given to certain problems concerning the transmission of data-type signals over the repeatered lines. The applicability of the present design is developed with relation to the short-haul plant.

I. INTRODUCTION

Since its manufacturing began in 1962, the T1 Carrier System[1] has been widely accepted by Bell System operating companies as an economic system of high performance for the transmission of voice signals in interoffice trunks. Although its use is growing and will continue to grow for voice transmission, it is significant that the T1 carrier regenerative repeatered line[2] witb its 1.544 megabit per second transmission capability is introducing into the Bell System tbe first common carrier high-speed digital transmission facility. Its potential use as a facility for the growing market of wideband data transmission is apparent.

Because the T1 carrier system was primarily developed for interoffice trunks of the exchange and toll connecting type its repeatered line design has been optimized for comparatively short haul use from the standpoint of the economics of installation and maintenance. Although distances of 200 miles or more may be obtainable, repeatered line installations have generally not exceeded 50 miles. Thus, it may be expected that initial use of T1 carrier as a wideband data facility will be emphasized for two general applications:

(i) As an extension of interexchange wideband circuits into the exchange plant, and

(ii) In the provision of very limited networks for the transmission of very high speed data for certain special uses.

Wideband data covers a broad category of data signals requiring transmission bandwidths greater than those of voice facilities. With the exception of TV, program, and some special, limited government services, demands for wideband data services did not materially develop until about 1958. At this time requirements for government services expanded and an interest in commercial transmission of computer type of data developed.

To date, about one million equivalent voice channel miles of wideband services have been furnished by the Bell System and their signal formats have been of a wide variety, including analog video, two-level facsimile, synchronous and asynchronous serial data, and parallel tape-to-tape and tape-to-computer data. To meet this variety of requirements initially, a number of special terminals were developed on an accelerated design and manufacturing schedule. It was clear, however, that for a continued expansion of wideband services an organized arrangement of standard offerings must be developed.

A large number of the signals transmitted over the present facilities may be resolved into a class of two-level serial signals which include synchronous serial data, asynchronous data, and facsimile. The following equipment has been developed or is in the process of development to provide for these types of services at data rates corresponding to group band and to supergroup band transmission:

(i) Data sets for processing machine information into a standard baseband format.

(ii) Modems for N carrier, L carrier and T1 carrier to process these baseband signals into the carrier facilities.

(iii) Baseband repeater systems utilizing wire pairs for interconnecting the data set at the customer's location to the telephone office.

II. SYSTEM OBJECTIVES FOR T1 CARRIER DATA TERMINALS

A prime objective in the design of data terminals for the T1 carrier system is that the line signal generated by these terminals be compatible with the existing T1 carrier regenerative repeatered line so that a line may be used interchangeably with a D1 bank signal or a data signal and that these signals may exist simultaneously in the same cable cross-section. Thus, consideration must be given to the pattern or format of the line signal generated by data terminals with at least two constraints. First, the character of the pattern on the line, including period and density, must not adversely affect other repeatered

lines through cable crosstalk; and second, the pattern must contain a sufficient number of pulses to maintain timing in the individual repeater clocks. Detailed requirements for the line signal as to level, impedance, bit rate and general format are well defined in the T1 carrier system.

Unfortunately, the requirements for the data signal to be transmitted cannot be as well defined. Even in respect to two-level serial signals, where some standardization is being attempted, the data rates are widely variable. In addition, many computer machines store and transfer data in the form of parallel words. In order to transpose these data signals into serial streams additional equipment is needed for "buffering" and word organization. It can be shown that in the case of T1 carrier it may be more efficient to inject these signals into the transmission system in the original parallel form, thus giving another general set of data signal requirements. Two specific designs of terminals will be described which accept some forms of data signals in these general classifications. In order to find general application, the terminals require a high degree of flexibility as to the form the input data signal can take.

The terminals will also require the capability of time division multiplexing a number of data signals together on one T1 carrier line when each signal does not fully utilize the line capabilities. When the number of data signals of any one type or rate is not large, it may also be desirable to multiplex different types of data signals together or even data signals with voice signals from the D1 bank. The system requirements for these capabilities are considered in the design of the terminals.

III. EQUIPMENT OBJECTIVES

Wideband data banks and modems are generally going to be installed in the telephone company central office. In addition, equipment designed to operate with a particular system, such as T1 carrier, should be located near that system's terminals. These premises imply that the equipment format should be chosen to be compatible with that of the "host" system.

The circuits which are being designed for the T1 carrier wideband data banks and modems are fashioned after existing D1 bank circuits. As a matter of fact, many of the timing circuits for the data terminals are identical to those used in the D1 bank. These factors, coupled with others developed earlier in this section, resulted in an examination of the consequences of using D1 bank hardware for the data terminals.

There are several advantages in adopting the D1 bank equipment

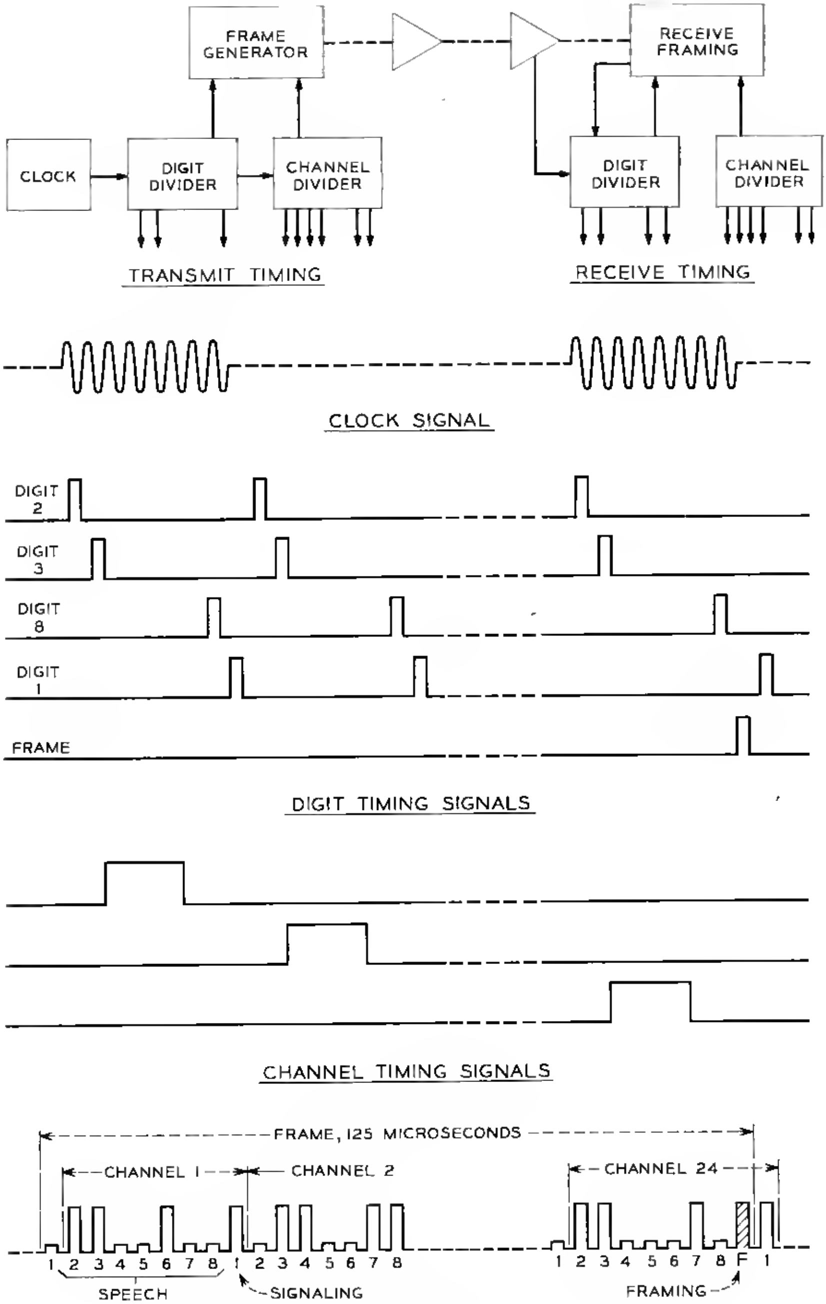


Fig. 1 — Block and timing diagrams for T1 carrier.

arrangements for data applications. Since, as already mentioned, the data terminals should be compatible with their voice terminal counterparts, the choice of existing D1 bank shelf castings and die-cast unit frames for data is a major step in achieving this compatibility. In addition, since the T1 carrier system is a high-production system, with some 130,000 group plug-in units shipped annually, distinct economic advantages are realizable by using the common piece parts and plug-in units when possible for the wideband data terminals. These considerations lead to the decision to use the same basic equipment design as that used in the T1 carrier D1 banks for the T1 carrier wideband data banks and modems.

Although most of the wideband data equipment could be in the central office, some of it will be installed on customer's premises, such as a computation center. In these cases, enclosures to house the normally relay-rack mounted equipment may be required to be complementary to the customer's installation.

IV. TERMINAL DESIGN

4.1 *Timing*

The basic control system of a time division multiplex terminal is its set of timing circuits. In order to derive the economic benefits of using standard D1 bank networks where applicable it is desirable that the timing circuit arrangements be similar. Fig. 1 shows functionally the basic components of these circuits. A crystal oscillator (1.544 mcps) provides the basic clock frequency and its output is used throughout the terminal for phase control of the signals. A digit generator normally divides the clock frequency by eight and provides 8 space and time separated outputs at this subdivided rate. A channel counter further subdivides the rate of the digit generator by 24, providing 24 space and time separated outputs, each at an 8-kc rate. For every 24th count of the channel counter (every 125 microseconds) the digit generator is controlled to count 9 instead of 8. This time slot contains a framing signal on the T1 carrier line whose function is to identify to the receiving timing circuits its unique position and thus the position of each of the 193 bits in every 125-microseconds frame period of the line signal. The receiver contains a clock which is controlled by the line signal to be synchronous with the oscillator in the transmitter. Dividers similar to those in the transmitting timing and framing logic circuitry provide a set of timing signals in the receiver identifiable with those generated in the transmitter.

In the D1 bank, the 24 voice input signals are each sampled in sequence every 125-microseconds frame period. These time divided samples are combined and each is sequentially coded into a 7-bit word by a common encoder circuit. An eighth bit is then added to each code word for signalling. It is natural, therefore, to find the eight bits of each sample grouped into words as shown in Fig. 1. It is neither natural nor convenient to force data signals into this format when time division multiplexing since it is desirable to provide in the bit stream equal sampling intervals for a channel. The periods of these intervals depend upon the number of T1 carrier line bits allocated to each channel. For example, assume a channel has been allocated one-half the repeatered line capability for transmission of its data signal. The timing for this channel can be controlled naturally from the timing derived from alternate line digits. Further, a channel requiring one eighth of the line can be controlled by a timing signal derived from every eighth digit. Since each of the 193 bits of a frame is uniquely identified, a variety of timing arrangements can be made using arrangements of the existing D1 bank circuitry.

4.2 *Serial Data Terminal*

One important application of data on T1 carrier will be as an extension of wideband toll data circuits through the exchange and local loop plants. For this a very flexible terminal is required to handle a variety of types of signals. Even if limited to two-level serial data signals this variety includes synchronous serial data of various rates, asynchronous serial data, and two-level facsimile. These signals may be considered as a class whose transitions between two levels occur at random with the minimum interval between transitions limited by the maximum data rate. The essential information to be transmitted for these signals is the time of transition and the state (1 or 0) after the transition.

Because the T1 carrier line is a synchronous digital facility, the analog information of transition time must be quantized and encoded in some manner. In the terminal design developed for this application these functions are accomplished efficiently with comparatively simple circuitry, meeting a maximum quantizing error objective of less than ± 10 per cent of the minimum data bit interval.

The principle of the "sliding index" provides the basis for the method of timing encoding in this terminal as well as the parallel data terminal to be described later. This principle was originally applied by Messrs. C. G. Davis and L. C. Thomas in the design of a parallel tape-to-computer data terminal for a dedicated T1 carrier line.[3] The essen-

tial feature of the "sliding index" approach is that it allows the insertion of a data word into a bit stream with the first available bit in the stream rather than holding the data for a particular position in the frame of the line signal. The details of the process will become more apparent in the following descriptions.

Consider first the simple functional block and timing diagram of Fig. 2. Line A shows a timing signal which is derived from clock and timing circuitry. As described earlier, this marks the time slots available in the T1 carrier line signal for one of a number of multiplexed data signals and may be every 2nd or every 8th or every nth bit as selected. Line B shows the data signal as applied to the terminal coder with transitions randomly distributed among the timing periods. In the absence of transitions the coder output is zero in the selected time slots (line C). When a transition occurs the next available time slot is indexed with a *ONE*, transmitting to the receiver decoder information that a transition has occurred between this time slot and the last preceding one. The coder then marks the next successive time slot with a *ONE* if the transition occurred in the early half of this period or a *ZERO* if it occurred in the late half. The third successive time slot is

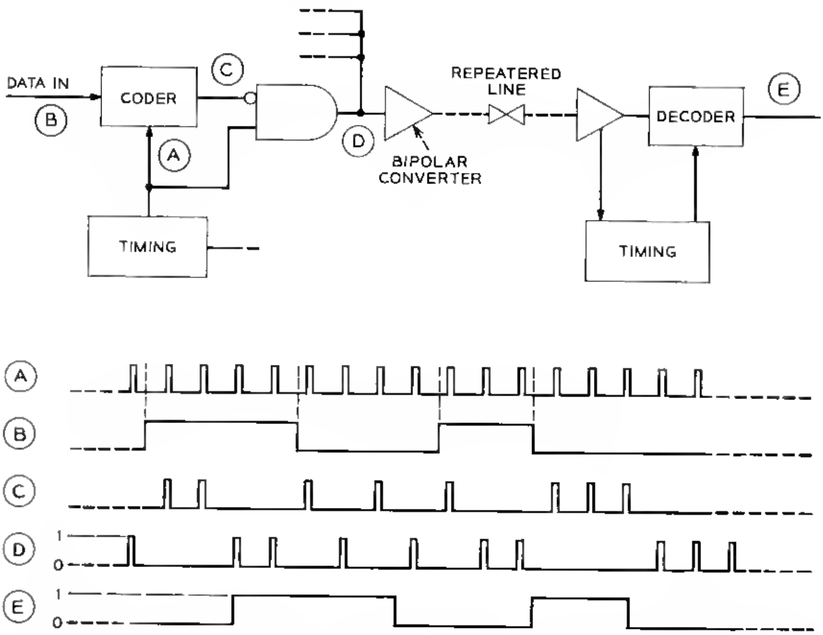


Fig. 2 — Functional block and timing diagram for the serial data terminal logic.

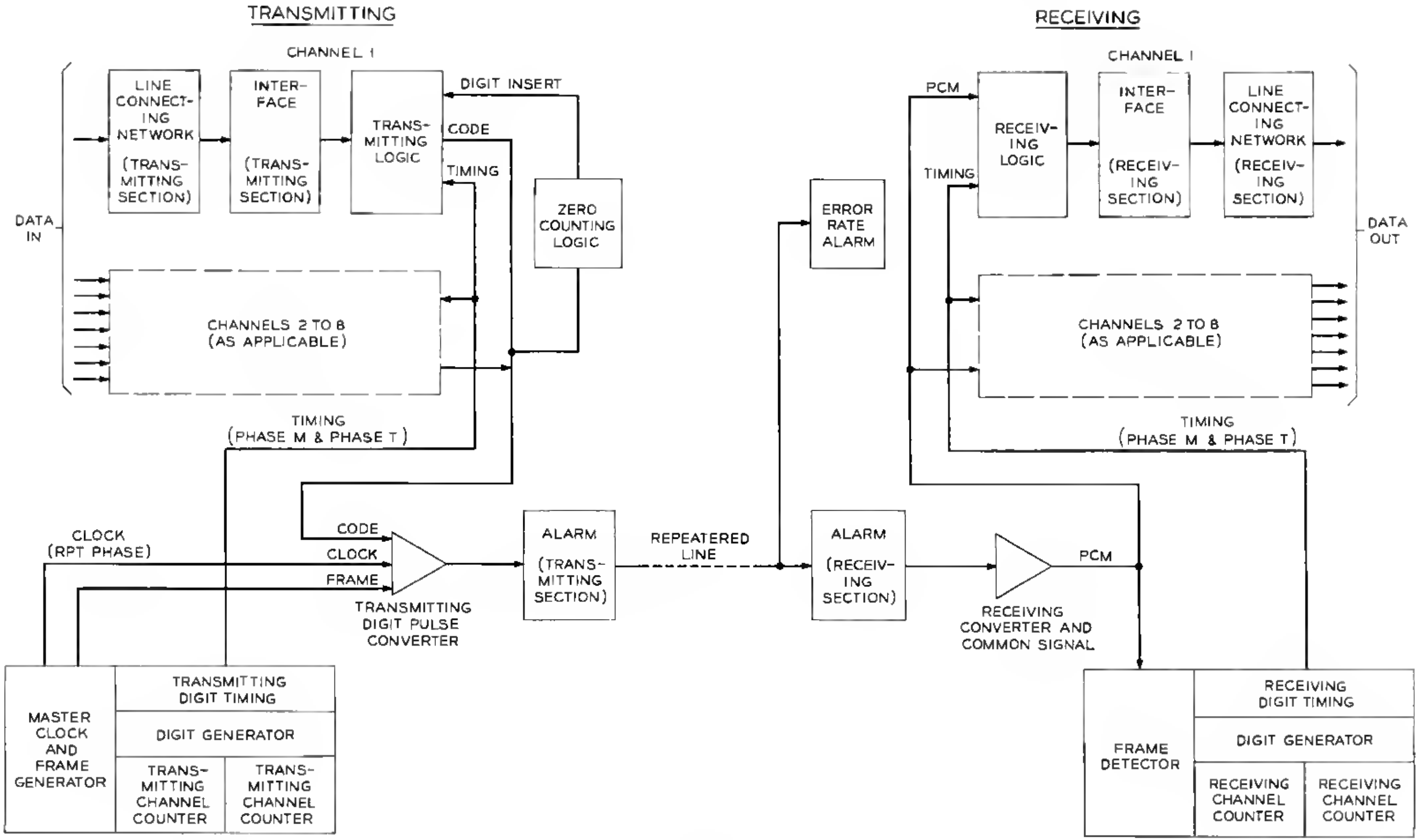


Fig. 3 — Block diagram of T1WB-1.

marked with a *ZERO* for a data transition from *ZERO* to *ONE* or a *ONE* for a transition from *ONE* to *ZERO*.

It should be noted here that if this output signal is logically inverted, then *ONES* will be transmitted in the absence of transitions. In general, this inversion is made because it provides a better timing signal on the line for the repeater clock circuits (line D).

The receiver decoder logic resolves this information into a data transition occurring within one-half of the selected timing interval plus a fixed delay. Since the minimum interval between data transitions must be limited to three selected T1 carrier timing intervals, and the transition is quantized to within $\frac{1}{2}$ this selected timing interval, the quantizing error is a maximum of $\pm\frac{1}{12}$ or ± 8.3 per cent, of this minimum data transition interval.

The foregoing is the process which is the basis for a set of data channel banks for asynchronous serial data transmission over T1 carrier lines. A number of functions must be performed in the terminals in addition to the coding process. Fig. 3 shows a block diagram of a data channel bank for up to 8 independent data signal inputs and includes the circuits for these auxiliary functions.

The arrangement of the timing circuits and their functions have been described in the general section on timing. In this 8-channel circuit specifically a digit timing unit is provided which steers the proper timing signals to each of the channel logic circuits such that the coded data signal for Channel 1 is transmitted in the time slot of Digit 1 on the line (Fig. 1), the data signal for Channel 2 in the time slot of Digit 2 and so forth.

In the coding process described earlier the data input was idealized as a two-level signal. The data signal received by the terminal as part of the standard wideband network will require amplitude regeneration to obtain this signal for several reasons. First, the data set processes the two-level signal as received from the customer's machine by removing low frequency energy from the signal in a controlled manner.[4] This is done to facilitate transmission over the analog facilities. In addition, the signal spectrum may be band limited and noise may be added in these facilities. The purpose of the transmitting Line Connecting Network and the Interface Network is to regenerate this signal to the two-level format. In some analog facilities, such as those including L-Multiplex, the frequency band for the data signal is limited to less than the bit rate frequency. For optimum shaping of the data signal prior to detection, a Line Connecting Network is provided which includes a network to roll off the band to a frequency 50 per cent above the signalling rate

or to $\frac{3}{4}$ the bit rate frequency. When the intervening facilities do not restrict the band tbis severely, as in the case of baseband repeatered lines, a second optional network is provided wbicb rolls off the band to 100 per cent above the signalling rate or to the bit rate frequency. These networks employ transfer functions which satisfy Nyquist's criteria for periodic zero crossings in the pulse response. When the data terminal is located near the data set such that little noise is added to the signal no shaping or roll-off network is required.

The Interface Network detects and regenerates this signal by first restoring its dc and low frequency components by means of quantized feedback, then slicing it. At the receiving end the Interface and Line Connecting Networks remove the low frequency energy from the signal to the same extent as the data set, thus preparing it for transmission through other facilities.

The combined outputs of the logic circuits consist of a stream of unipolar pulses. These are applied to a Digit Pulse Converter whose function is to alternate the pulses from plus to minus creating the bipolar pulse stream required for the T1 carrier line. The receiving converter derives the basic clock signal from tbis pulse stream and converts the received signal back to its unipolar format. This unipolar signal is applied to all receiving logic circuits where it is demultiplexed by the timing signals and decoded.

Two alarm arrangements are provided. One circuit presents an alarm when framing is lost in the receiving bank. Its features are similar to tbose provided in the D1 bank, including the capability of terminal looping. However, the T1 carrier framing circuits are comparatively rugged and require error rates in the order of 10^{-3} in order to initiate an alarm. For this reason a second alarm circuit is provided which alarms directly on line error rate. This circuit includes a bipolar violation detector which provides a measure of line errors. By means of an integrating circuit an alarm indication is obtained when the error rate exceeds a predetermined value, say 10^{-6}.

Due to the inherent flexibility of time division multiplex systems, only minor changes in timing arrangements are required to obtain a variety of data speed options. For example, if the timing signal is arranged to code an asynchronous data signal into every eighth T1 carrier bit, this channel will have a maximum data rate capability of 64 kilobits per second, adequate for the 50-kilobit signals to be transmitted in the group band over L-multiplex toll facilities. Eight such signals can be multiplexed on one T1 carrier line. Further, data rates up to 256 kilobits per second may be transmitted over a channel whose

signals are coded into every second T1 carrier bit, providing a capability corresponding to supergroup transmission in L Multiplex. Table I lists some typical asynchronous serial data rates with their limits of timing error due to quantizing.

The framing time slot in the line signal introduces an additional timing error which is not included in Table I. This error occurs when a transition is such that its 3-bit code sequence encompasses the framing time slot; it introduces an additional timing delay of 0.6 microseconds. This is significant for the case of 256 kilobits/second data transmission, but only occurs on about 2 per cent of the transitions. A number of subjective tests have been made transmitting facsimile copy at this rate. No apparent degradation in performance occurred which could be attributed to the framing error. If further tests and field experience show this error to be of some importance additional logic circuitry may be added to constrain this error to occur only when the data transition occurs during the framing time slot, or about 0.5 per cent of the transitions.

4.3 *T1WB-1 and T1WB-2 Wideband Bank Equipment Design*

The first standard offerings for wideband data terminals for T1 carrier, based upon the foregoing discussion, are the T1WB-1 and T1WB-2 wideband banks. The banks are made up of die-cast aluminum shelves which mount the plug-in timing, logic, line connecting and interface units, and fabricated panels which contain other line connecting and miscellaneous circuits. Figs. 4 and 5 illustrate the use of T1 carrier hardware in these banks.

The two banks described here differ only in their respective data channel capacities. The T1WB-1 wideband bank is arranged to transmit and receive up to eight two-level asynchronous serial data or facsimile signals over a T1 carrier repeatered line. The T1WB-2 wideband bank is a scaled-down version, being arranged to process up to two 250-kilobit signals.

TABLE I

T1 Line Loading	Number of Channels Per Line	Max. Data Rate In kb Per Sec.	Max. Timing Error
1/8	8	64	±1.3 Microseconds
1/4	4	128	±0.65 Microseconds
1/2	2	256	±0.35 Microseconds
1/1	1	512	±0.17 Microseconds

FIG. 4 — T1WB-1.

Hardware in the banks has been grouped into two categories. The equipment for processing the customer's baseband signal into a PCM signal is termed channel equipment. This equipment can be plugged into the terminal on a per customer basis. Equipment which is shared by all channels to derive timing information and to provide fuse and alarm indications is termed common equipment. A portion of this latter equipment consists of panel mounted jacks, battery filters and terminal strips for access to the banks. The remainder, the active circuitry, is

provided as plug-in units. The two banks make use of similar configurations of these equipments as may be seen in Figs. 4 and 5.

The T1WB-1 wideband bank occupies a space of nineteen $1\frac{3}{4}$-inch by 23-inch mounting plates and weighs 130 pounds when fully equipped. The T1WB-2 occupies a space of thirteen $1\frac{3}{4}$-inch by 23-inch mounting plates and weighs 80 pounds when fully equipped. The banks may be mounted on 10-inch deep bulb angle bay frameworks or 12-inch deep cable duct bay frameworks. All installer wiring is brought to terminal strips on the rear of the banks. This, of course, means that no back-to-back bay lineups are possible for T1 carrier wideband data installations. However, the same restriction exists for the T1 carrier voice terminal.

Since both banks are functionally and mechanically similar except as outlined above, further description will not be identified with either bank. Unless otherwise stated, comments made will apply to both.

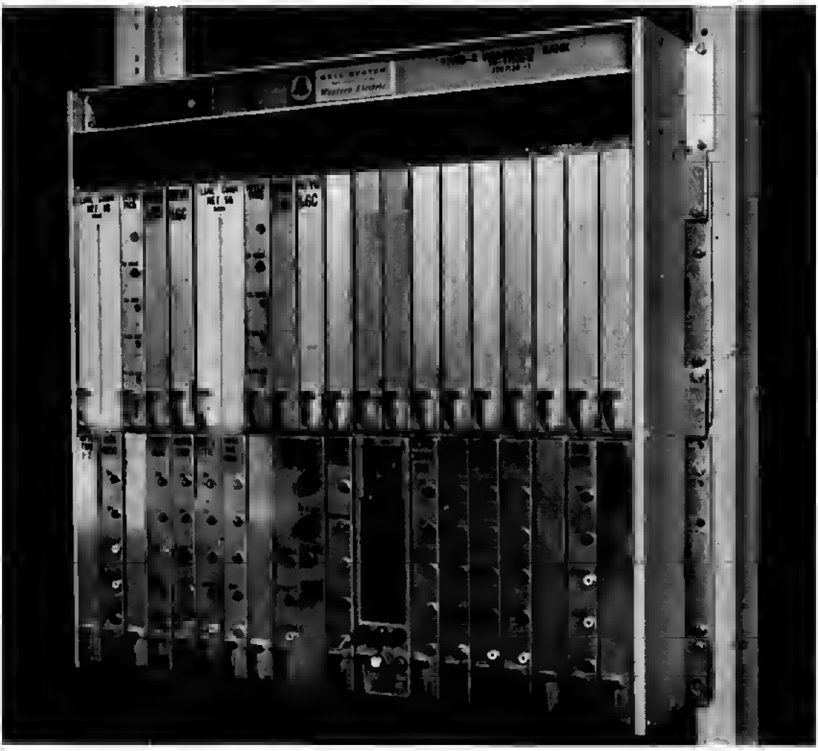


Fig. 5 — T1WB-2.

The timing and channel shelf assemblies consist of die-cast aluminum piece parts bolted together in such a way as to accept the plug-in units. Fig. 6 shows an assembly of two shelves. It may be noted that the assembly consists of two connector mounting die castings and three other die castings which contain the tracks and retaining slots into which the plug-in units slide and lock in place. The entire assembly is strengthened by dividers which also serve as interposition shields. The connector mounting die casting is designed to hold up to twenty pairs of connectors, each pair mounted one vertically over the other as shown. This connector arrangement provides a maximum of forty-two terminals for each plug-in unit. One shelf assembly can be equipped with twenty "single" plug-in units or ten "double" plug-in units or combinations of the two types. The connector-mounting die casting has mounting holes on the rear for attaching terminal strips.

Typical plug-in units are shown in Fig. 7, one the "single" type and the other the "double" type. Either unit is made up of a die-cast aluminum frame, a printed wiring board and one or two plugs. The

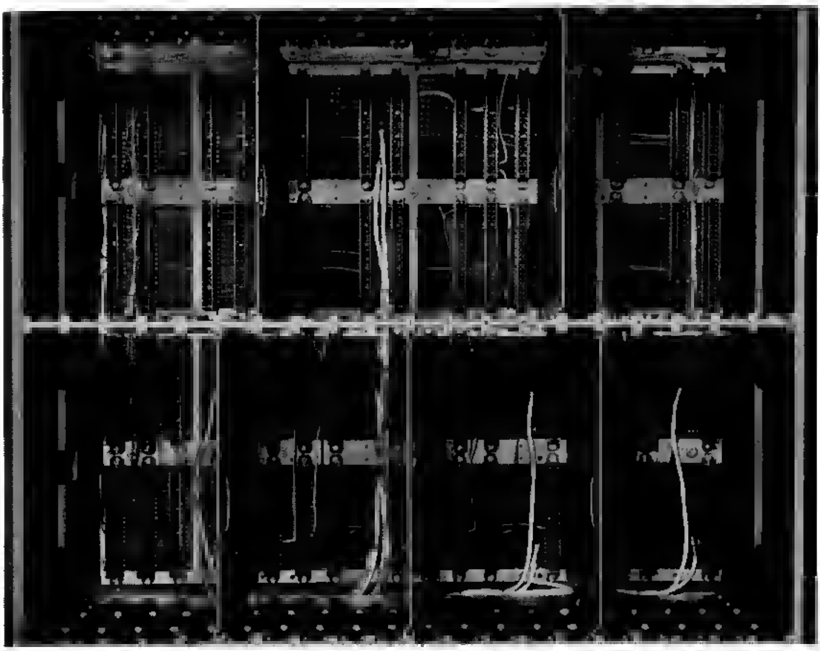


Fig. 6 — Typical shelf assembly showing type of construction and placement of connectors.

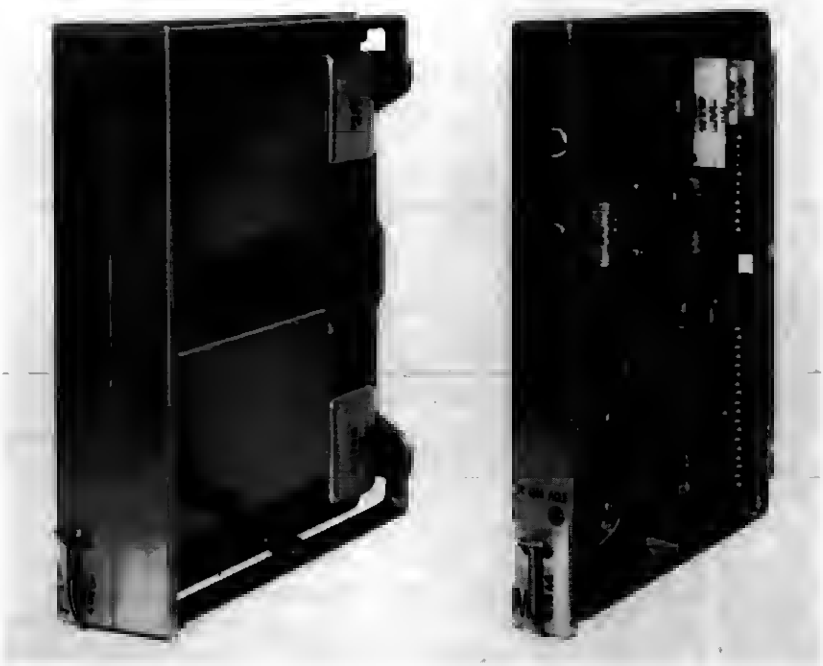


Fig. 7 — Typical T1WB-1 or T1WB-2 plug-in units.

frame has a latch mechanism not unlike others used in the telephone plant which locks the unit in place when inserted into the shelf assembly. The latch also serves to break the connector contact pressure when the unit is to be extracted. The printed wiring board is either of a fire retardent phenol fiber material or an epoxy glass material depending upon the mass of the component apparatus to be mounted upon it. It may be double-sided or single-sided depending upon the complexity of the circuit. In the double-sided case, connections between sides of the board are provided by through-straps. The over-all dimensions of the single plug-in units are approximately $8\frac{5}{8}$ inches by $7\frac{29}{32}$ inches by 1 inch, exclusive of the latch and plug. The double plug-in units are approximately $8\frac{5}{8}$ inches by $7\frac{29}{32}$ inches by 2 inches, exclusive of the latch and plug.

Out of 27 separate codes of plug-in units required for all modes of operation of the T1WB-1 and T1WB-2 wideband banks, 7 are already used in the T1 carrier system. The 20 new codes were designed using

the same types of components used in T1 carrier whenever possible. In addition, no new assembly techniques have been introduced which might incur retraining of shop personnel.

The line connector panels deviate from the T1 carrier hardware. These panels are fabricated assemblies of 0.090-inch sheet aluminum. They mount power filters, terminal strips and access jacks for the baseband channels. In addition, sockets are mounted on these panels for plug-in span pads. Fig. 8 shows the two line connector panels required for the T1WB-1 wideband bank. The top panel is also used for the T1WB-2.

Let us now explore the operational features of the banks. The T1WB-1 and T1WB-2 wideband banks have been designed to provide optimum flexibility in the treatment of two-level asynchronous serial data or facsimile signals over a wide range of data rates. The flexibility required was attained by design in the common circuits for practical combinations of these signals. This resulted in an equipment arrangement unhindered by wiring options necessary for the field to modify as data signal requirements changed. Administering the various possible combinations of signals now becomes simply a choice of plug-in units. Table II shows the available combinations.

Plug-in units, inserted on a per channel basis, serve to prepare the baseband data signal for its insertion onto the T1 carrier repeatered line. Different data rates and the necessary baseband line equalization are achieved by selecting the proper plug-in units. In addition, other

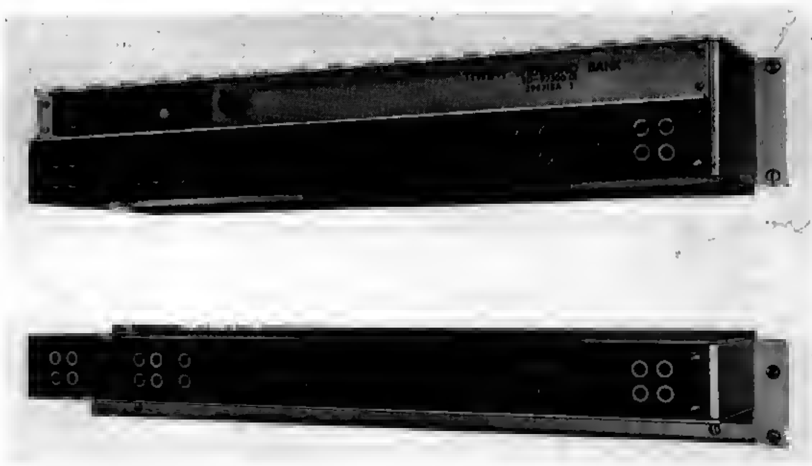


FIG. 8 — Line connector panels.

TABLE II

Wideband Bank	Multiplex
T1WB-1	8 channel — 50 kb
	4 channel — 50 kb 1 channel — 250 kb
	2 channel — 250 kb
T1WB-2	2 channel — 250 kb

units are available to limit the number of successive *ZEROS* in the line signal for satisfactory repeater operation. Timing for the data bank is provided by another group of plug-in units.

The T1WB-1 and T1WB-2 wideband banks are equipped with optional pads or equalizers to compensate for the cable length between the bank and the T1 carrier office repeater. This is a wired option, since it is considered unlikely that, once installed, it will have to be changed.

If the data bank is installed in a location having no other T1 carrier facilities, auxiliary panels are provided. These panels mount the necessary equipment for connecting the bank to a repeatered line and for fault locating on that line. Panel designs are available in the T1 carrier system to perform these functions.

The T1 carrier system may provide a very convenient means for interconnection of central office equipment and a data set at a customer's location even though the repeatered line is dedicated to a single data signal. For these applications, the T1WM-1 wideband modem has been developed which is basically a simplified version of the T1WB-1 and -2 banks. It consists of a single shelf of plug-in networks similar to those used in the banks. However, most of the timing units required for multiplexing and framing are eliminated. This modem is capable of transmitting serial data signals up to 500-kilobit rates.

4.4 *Terminals for Parallel Data*

The geographical diversification of large research and development organizations with a common need for high-speed computer facilities creates a requirement for data transmission at rates above those generally required for business machine data or facsimile. One example of such a complex is represented by three major Bell Telephone Laboratories locations at Murray Hill, Holmdel and Whippany, New Jersey. Each of these locations contains a computation center equipped with

large, high-speed computer facilities. The need for load sharing, during heavy load periods or computer "down time" at one location, is but one reason for interconnecting these centers with data transmission facilities. Because of its obvious convenience for experimentation and testing, this Laboratories' computer complex was selected as a model for the development of experimental T1 carrier data terminals for this general type of service. It will be shown, however, that the basic design contains sufficient flexibility to operate with a large variety of computer systems.

The interchange of information in the present Bell Laboratories' computer complex principally involves tape machine to tape machine or tape machine to computer data transmission. Fig. 9 shows the essential units for this operation when the transmitting tape machine is remotely located. Under the control of slow speed signals sent from the receiving equipment the tape machine reads data from the tape, transmitting it to the data terminal in the form of groups of parallel data characters. The data terminal puts this information into a form suitable for transmission over a T1 carrier line and restores it to the original parallel character format at the receiving end.

The character size, that is the number of bits per character, and the character rate are dependent upon a particular tape machine design. In the Bell Laboratories service tape machines are used which transmit a 7-bit (or 7-level) character at nominal rates up to 90 kilocharacters per second. Because of the nature of tape drive mechanisms this character rate is somewhat "elastic" and may have momentary variations as great as ±20 per cent of the nominal rate. It is important, however, that the character spacing be preserved in transmission within some

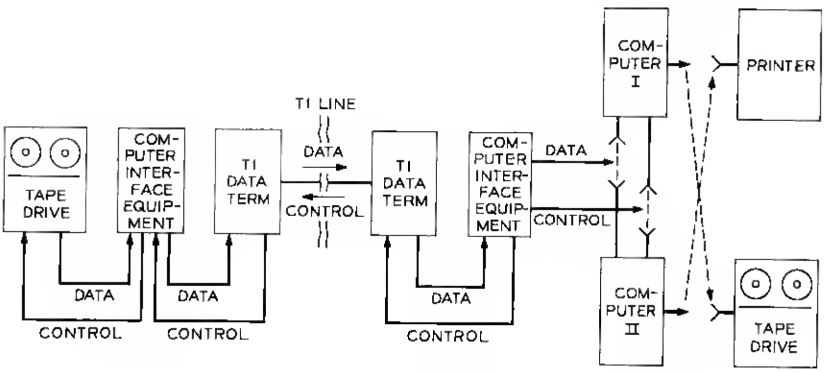


Fig. 9 — Remote computer control operation block diagram.

limitation since this spacing may contain information essential to receiving computer equipment. Since much of the character spacing tolerance is used up in tape speed variation, little is left for the transmission system. The principal point to be made here is that T1 carrier data terminals must be capable of transmitting these signals at asynchronous character rates while quantizing the character timing information within about ± 15 per cent of the minimum character period.

In general, the prior discussion of terminal timing control for serial data terminals is also applicable to the parallel data terminal. However, because of the data rates involved, the terminal has been designed principally for a dedicated data service with the multiplexing capability used for auxiliary signals such as the slow speed control signals. The block diagram of Fig. 10 shows circuits which generate a set of timing signals including framing. Of this set of signals the data clock signal controls the timing of the input data signals and marks the bit intervals on the line in which the data signals are transmitted. As shown in the timing diagram, Fig. 11, these bit intervals consist of all but the framing time slot and those selected for the auxiliary control information. In the absence of data input signals *ONES* are transmitted on the T1 carrier line in these time slots.

The data characters are transmitted to the terminal from the computer equipment on seven parallel leads, each lead handling one bit of the character in a bipolar format of plus and minus pulses for *ONES* and no signal for *ZEROS*. A data character is recognized when a pulse (a *ONE*) is transmitted on any one or more leads. On this event all leads are read and those with no pulses are considered to be transmitting *ZEROS*. No significance exists in the polarity of the pulses nor does any relation exist in the polarity of a pulse on one lead with respect to any other.

When a data character is transmitted to the terminal the pulses are rectified to a unipolar format and detected in the interface circuit. The detected signals are applied to respective stages of the register and the data character is stored there. The occurrence of the data character is also recognized by the data logic circuit which, on this occurrence, applies the data clock signal to the shift control of the register. This causes first a *ZERO* index to be transmitted on the line, followed immediately by the seven bits of the data character. Should a control or framing time slot occur during this interval, the shifting sequence will stop for that time slot, resuming its count after the auxiliary signal is transmitted.

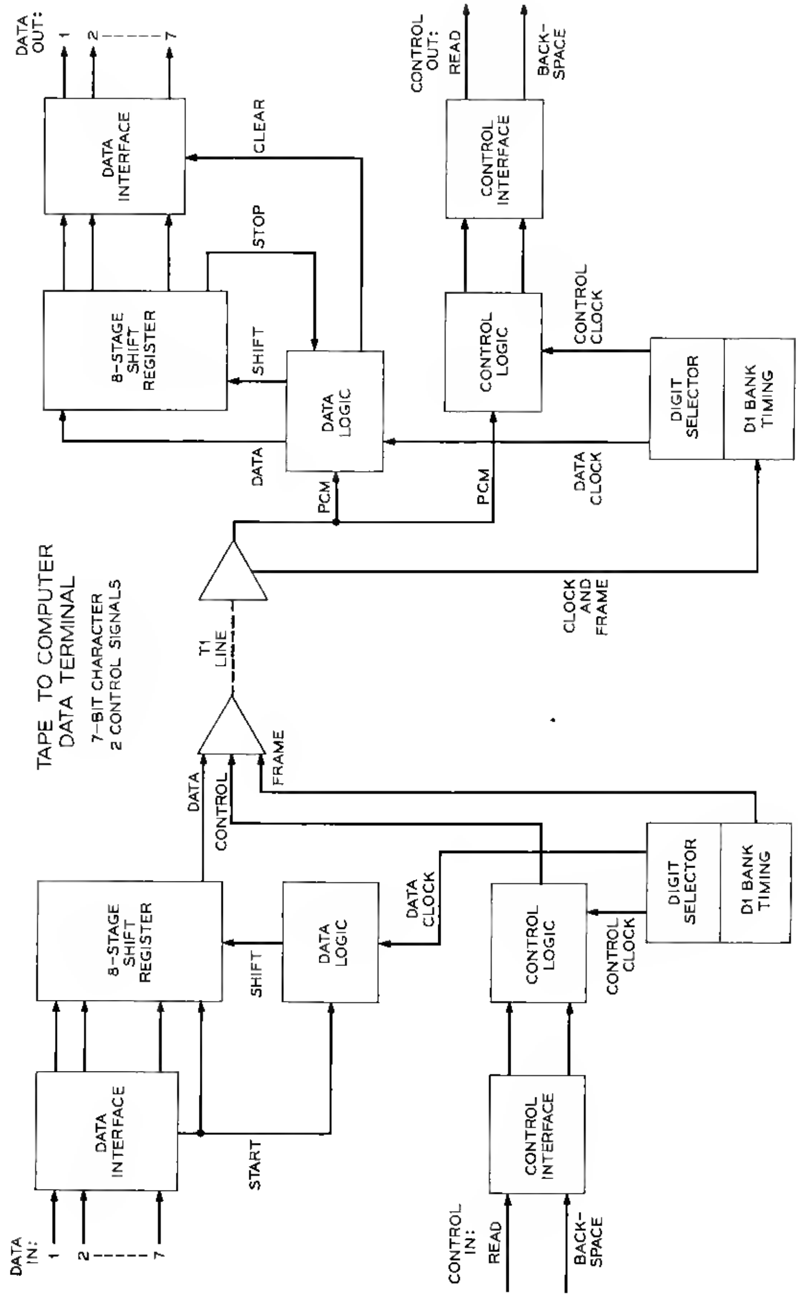


Fig. 10 — Block diagram for a parallel terminal.

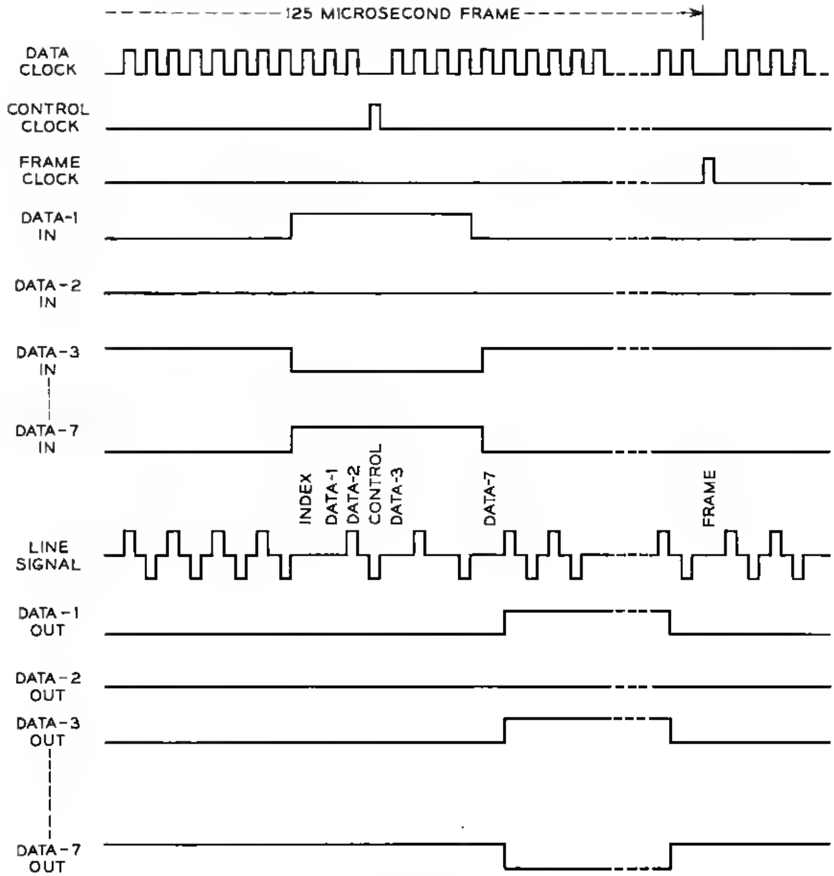


Fig. 11 — Timing diagram for a parallel terminal.

In the receiver, the *ZERO* index is recognized as the address of the character by the receiving data logic. This circuit then applies a data clock signal to the shift control of the register, causing the next seven data bits to be shifted into the register. This data clock signal is identical to and synchronized with that of the transmitter, and thus excludes the timing interval during which framing or control signals occur. When a control or framing bit occurs within a data word the shifting sequence stops for that interval allowing only bits of the data word to enter the register. At the end of the count, the shifting sequence is stopped and the data character is transferred in parallel form to the interface. The interface generates bipolar pulses for *ONES* in the character, ap-

plying them to the parallel leads for transmission to the computer equipment.

What has been shown so far is only half of the full-duplex capabilities of this data system. With both transmitting and receiving terminals at each end another set of independent parallel data signals may be sent in the opposite direction. Multiplexed with this set, however, are the slow speed control signals, alluded to earlier, for the first set of parallel data signals. These control signals are simple instructions or commands to the sending computer equipment and consist of binary impulses spaced not less than 6 to 8 milliseconds apart. A separate lead is supplied in the receiving computer equipment for each control signal required.

The coding and multiplexing of these control signals is rather easily implemented. For each control bit required, a T1 carrier bit is selected by the timing control from every 193-bit frame. The timing is so arranged that the control bits are approximately evenly distributed in the frame. In the absence of control data, *ONES* are transmitted on the line in these bit periods. When a control impulse is applied on one of the control inputs, *ZEROS* are transmitted in its particular bit period for three successive frames. Majority logic circuits in the receiver recognize this signal on a 2 out of 3 bit basis, providing for single bit error correction. From this information an impulse is regenerated and applied on the appropriate control lead to the computer equipment. Control impulses as closely spaced as 500 microseconds may be accommodated.

From the foregoing it may be seen readily that the character timing of the high speed data is preserved within the quantizing of the data timing signal. Except when the character is transmitted over a framing or control bit period the resulting distortion is within ± 0.33 microseconds. The framing or control bit will add 0.65 microseconds delay to characters encompassing their time slots. It may also be seen that the character size is not dependent upon the basic terminal design. By adding or removing certain stages of the terminal the character size capability may be increased or decreased with an inversely proportionate transmission rate capability. This is shown in the following relationship and summarized for some typical character sizes in Table III.

$$\text{Max. Char. Rate} = \frac{1544 - 8(C + 1)}{N + 1} \text{ kilocharacters per second}$$

where N is the number of bits per character, and C is the number of control channels.

TABLE III

Bits per Character	No. of Control Channels	Max. Character Rate	Nominal Timing Error in % of Min. Char. Interval*
12	4	115 kc	±3.8%
8	2	168 kc	±5.6%
4	2	304 kc	±10.0%

* Delay of framing or control bit is not included.

4.5 *Parallel Data Terminal Equipment*

A parallel data terminal has been implemented to process data characters up to 12 bits in length and as many as 6 control signals (see Fig. 12). This parallel data terminal consists of signal transforming equipment and common timing and alarm equipment. The modem occupies a space of eighteen $1\frac{3}{4}$-inch by 23-inch mounting plates and weighs approximately 130 pounds when fully equipped. It may be mounted on a 10-inch deep bulb angle bay framework or a 12-inch deep cable duct bay framework. As in the other T1 carrier data terminals, all the installer wiring is brought to terminal strips on the rear of the unit.

Continuing the philosophy that once the unit is installed, no further installer effort is required to make changes on it, the parallel terminal provides optional features on either a plug-in basis or a solderless wrap strap basis. Fig. 13 shows a rear view of the modem in which may be seen these strap options.

The construction of the shelves and panels is identical to that already described for the T1WB-1 and T1WB-2. Die-cast aluminum shelves and fabricated aluminum panels are the principal structural members. The plug-in units are single-sided and double-sided printed wiring boards mounted in die-cast aluminum unit frames. Fig. 14 shows a typical plug-in unit. This terminal makes use of "cord wood" component packages, as shown in Fig. 15, to derive a more efficient packing factor in its plug-in units. In the illustration, the "cord wood" module is a flip-flop having sufficient output leads to perform a variety of logic functions (see Fig. 16).

Although the modular concept is generally more expensive than the laying down of components directly to the printed wiring board, its use in this terminal has resulted in at least a 25 per cent reduction in total terminal volume. Conventional component placement would have required more plug-in units and, hence, another shelf to mount them.

This parallel data terminal provides flexibility of word size and the number of control channels in a unique manner. Fig. 17 illustrates how

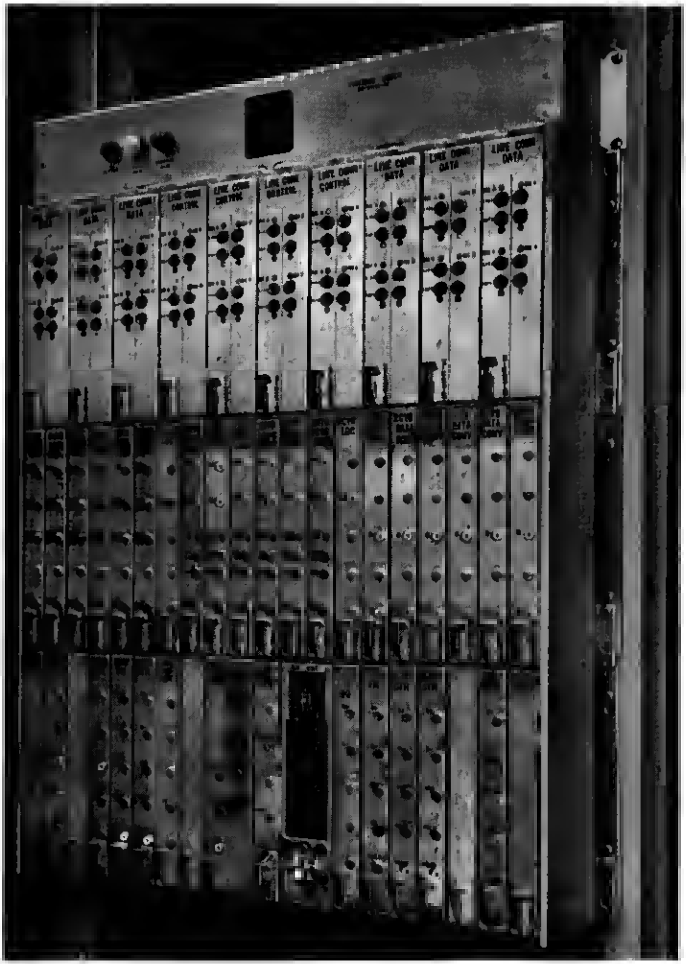


FIG. 12 — Parallel data terminal.

the transmitting side of the terminal is arranged for processing a 6- or an 8-bit character.

Plug-in units called Data Converters are each equipped with two separate interface circuits (I) and shift register stages (R). The shelf wiring is arranged to provide the unit interconnection as shown in the figure. A second type of plug-in unit called the Data Logic Unit is back wired to Data Converter 1.

As developed earlier, a pulse or *ONE* on any of the "bit" leads is recognized by the Data Logic unit via the "sense" lead and the register is read out serially.

The important thing to note here is that by plugging the proper number of data converters into the shelf and inserting the Data Logic unit into the slot next to the first Data Converter, any number of bits up to the capacity of the terminal may be accommodated. A strap option in the back wiring further provides for the handling of even or odd bit characters.

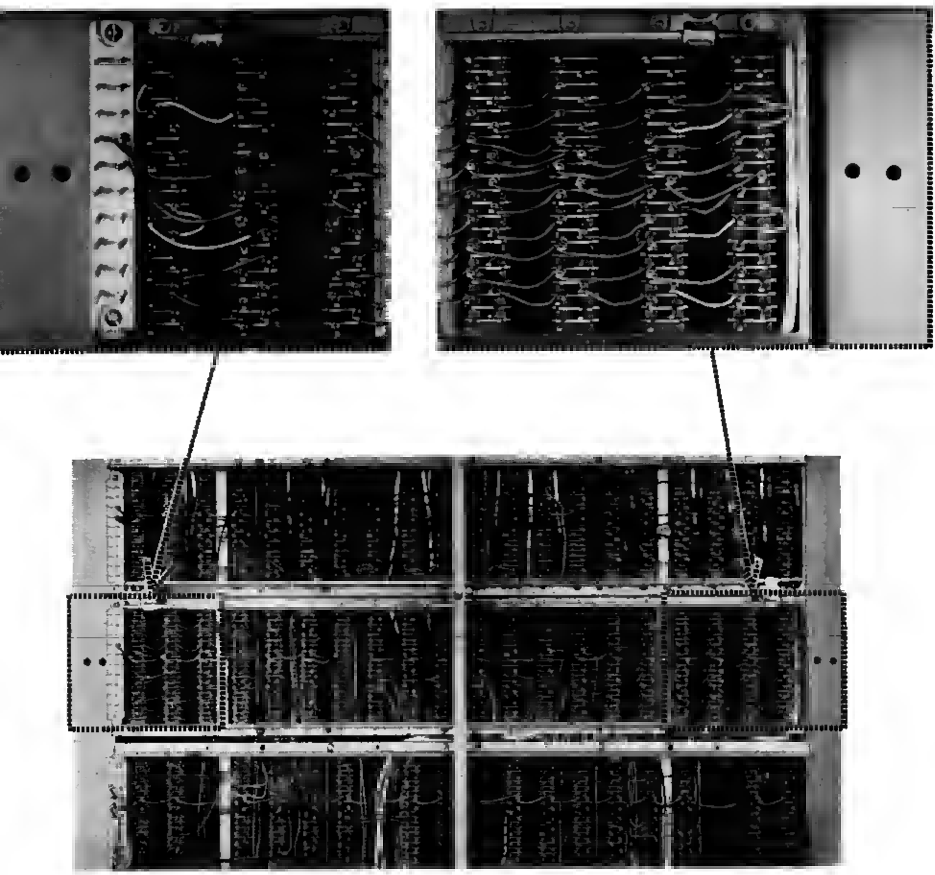


Fig. 13 — Rear view of parallel data terminal showing specifically the location of the strap options.

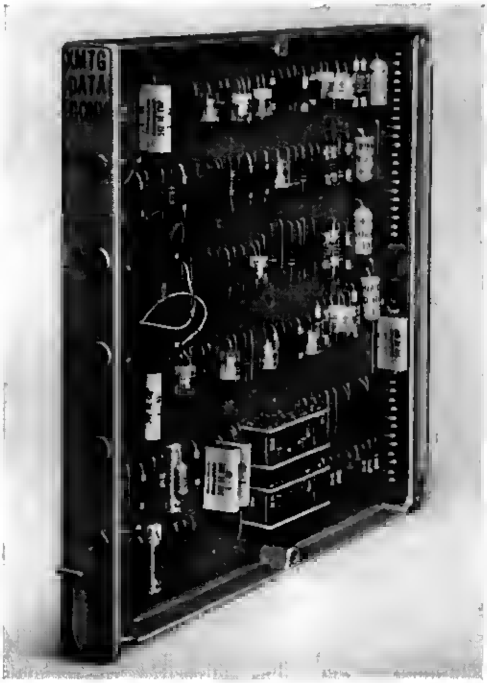


Fig. 14 — Typical parallel data terminal plug-in unit with "cord wood" modules in place.

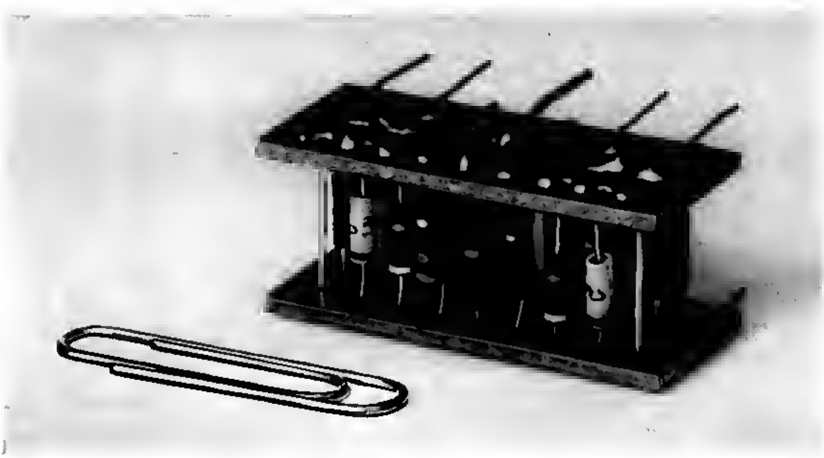


Fig. 15 — Flip-flop "cord wood" module.

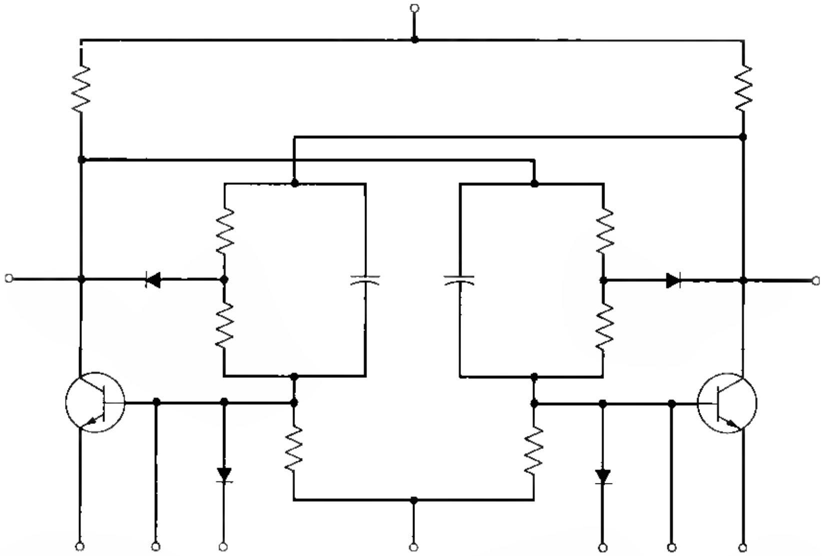


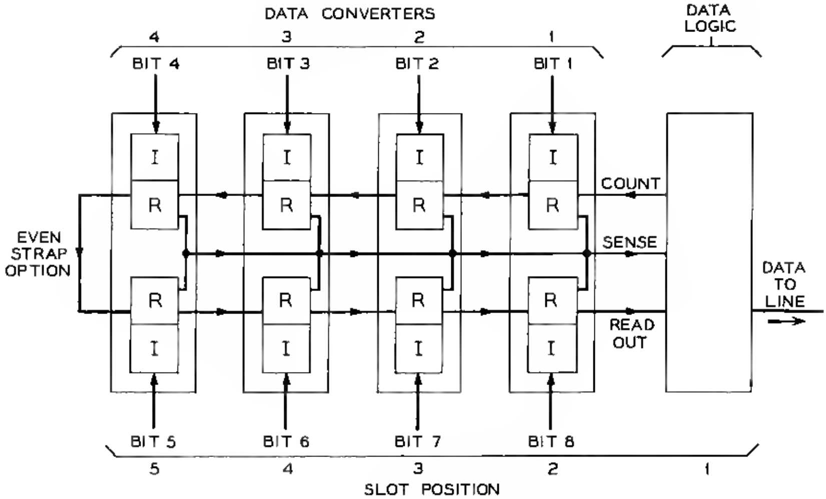
FIG. 16 — Schematic of flip-flop circuit which is packaged as "cord wood" module.

The receiving side of the terminal for data character processing uses the same mechanical implementation as does also the control channel circuitry.

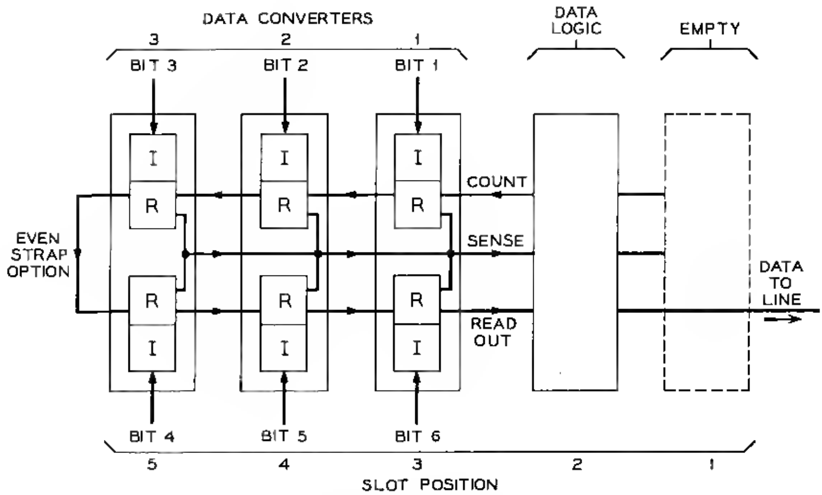
Fig. 18 shows the terminal arranged to transmit an 8-bit character and a 6-bit character plus control signals. Note the differences in the arrangement of plug-in converters and logic boards.

4.6 *Field Performance*

Since June of 1962, T1 carrier has provided for data transmission among the Bell Laboratories computation centers at Holmdel, Whippany and Murray Hill. This service requires transmission of the data over the distances of roughly 20, 40 and 60 miles. The system made possible the remote operation of the computers through the transmission of 7-level tape data at nominal speeds of 62.5 kilocharacters per second. It has been used primarily for load sharing among the locations. In the spring of 1963, laboratory models of terminals based on the design described above replaced earlier terminal equipment. After a period of shakedown of the terminals and the T1 carrier repeatered lines, the system reached and sustained reliable performance at very low error rates. Record retransmissions which result from transmission errors, have averaged about 0.01 per cent for 1000 character records, corresponding to an average T1 carrier line error rate of 10^{-8}. This per-



(a) EIGHT-BIT CHARACTER



(b) SIX-BIT CHARACTER

Fig. 17 — Block diagram of plug-in arrangement for data transmitting side.

Fig. 18 — Parallel data terminal arranged for (a) 8-bit characters and 2 control channels and (b) 6-bit characters and 4 control channels.

formance is approaching that obtained with a direct tape-to-computer connection.

During this time improvements and changes have been added to the terminal models. Recently both the computer and the terminal equipment were changed to operate at a nominal speed of 90 kilocharacters per second. In addition, changes were made to multiplex the control signals with the data. These control signals were previously transmitted over a separate voice facility.

The data shown on Fig. 19 is indicative of the usage of the network as it has developed over two years. They show the hours per month in computer time that the Murray Hill center received data for processing from the other two locations. The peak, in August, 1964, was the result of an extended down time period of the Holmdel computer for modifications. Recently a second computer and T1 carrier data terminal were added to the Holmdel center. An additional T1 carrier repeatered line facility was provided from Holmdel to Whippany. Terminal-to-line switching equipment allows flexible interconnection of the computers as shown in Fig. 20. It is estimated that for one interconnection alone the Holmdel center is processing at least one-half a computer shift (about 90 hours per month) of work originating at Whippany.

V. GENERAL DEVELOPMENT PROBLEMS

5.1 *Long "0" Sequence Control*

Several general problems arise in applying data signals to T1 carrier lines which must be considered in the design of terminals. One of the

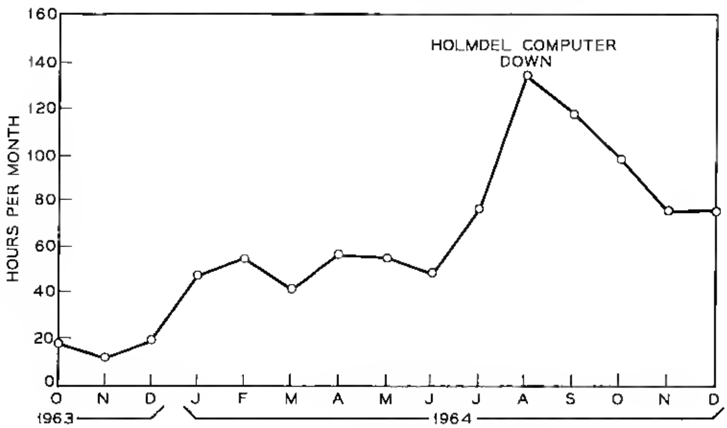


Fig. 19 — Data network usage.

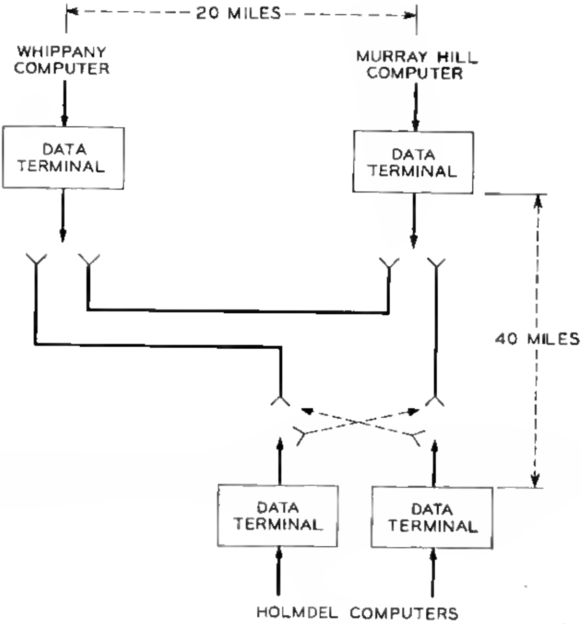


Fig. 20 — Data network layout.

most important relates to limiting long sequences of *ZEROS* in the line signal in order that the repeater clocks remain activated. A properly engineered T1 carrier line should normally tolerate a sequence of up to 14 clock periods without a pulse. In the D1 bank this sequence is limited by the suppression of the all *ZERO* word in the encoder at the loss of only one of the 128 coding levels. A data terminal will not have a similar direct control of the data sequence and other means must be arranged.

In the design of the T1WB-1 bank for asynchronous serial data, use was made of the statistics of the data signal and redundancy in the terminal coding process to control the *ZERO* sequence. Consider for this terminal that the input signals consist of eight statistically independent random binary data signals, synchronous at a 50-kilobit rate. For the worst limiting condition, each data signal has an equal probability of a *ONE* or a *ZERO* in any bit period. It can be shown that, without any constraint on the coding process of the T1WB-1 bank, the probability, P_m, of the occurrence of a continuous sequence of at least m *ZEROS* following a *ONE* is as follows:

m	P_m	*One Occurrence Every*
8	1.23×10^{-5}	0.05 sec.
10	1.90×10^{-6}	0.34 sec.
12	2.92×10^{-7}	2.2 sec.
14	4.50×10^{-8}	14.4 sec.

Although this is several orders of magnitude better than a purely random sequence applied directly on the line, the occurrence of 14 or more *ZEROS* and the likely loss of line synchronization every 15 seconds is not tolerable. A constraint has been added to the coding process of the bank, however, which considerably improves this condition. The Zero Counting Logic Network is provided which counts successive *ZEROS* in the T1 carrier line signal. This is essentially a binary counter which advances on every clock bit but is reset by any *ONE* being transmitted. At a count of 8 *ZEROS* the counter provides a control to all 8 channel logic circuits such that unless a *ONE* is first transmitted for any other reason, the next channel transmitting an "early-late" bit (the 2nd bit of the coding sequence) will transmit a *ONE* whether the transition is *early* or *late*. Forcing the code in this manner produces only a small error in timing but does not produce a complete data bit error. With this added constraint, the following probabilities result:

m	P_m	*One Occurrence Every*
8	1.23×10^{-5}	0.05 sec.
10	2.50×10^{-7}	2.6 sec.
12	5.07×10^{-9}	2.1 min.
14	1.03×10^{-10}	1.8 hours

It is expected that when the traffic statistics are included, a satisfactory line signal condition will result. Any other set of data signal characteristics, such as that resulting from a facsimile signal or the use of an Idle Channel Connector in place of an unequipped channel position, reduces the probability of a long *ZERO* sequence.

Because the statistics as to word format and data rate are more favorable, no *ZERO* sequence control has been incorporated in the design of the terminal for parallel data. This problem can exist only when two successive characters contain an arrangement of 14 or more consecutive *ZEROS* (i.e. 10000000,00000001) and are spaced at the minimum character interval such that no idle line bit (a *ONE* on the line) is transmitted between them. It would be possible, however, to eliminate even this condition by incorporating circuitry which would force an idle line bit between the characters when this condition is anticipated.

These methods of *ZERO* sequence control are dependent on the

particular terminal design and the statistics of the data input signals. Terminal designs for parallel data with large size characters, say 36 bits, or for terminals for hybrid combinations of data and voice signals on one line may require different methods of control. For this reason, consideration is being given to more general arrangements. One method requires that every nth bit, say every 12th bit, on the line be allocated for control purposes. This would result, of course, in a proportionate reduction in data capacity. These bits may be used, however, for auxiliary terminal control functions such as alarm or order wire, or for the transmission of slow speed error control information.

Another method, which may not necessarily reduce the data rate capacity, involves the recoding of the line signal to other than the bipolar format. Although the repeatered line was primarily designed for bipolar signals it has the capability of transmitting ternary signals with certain constraints as to the sequence of pulses of one polarity. Falling somewhat within these constraints is the Paired Selected Ternary (PST) code[5] developed for an experimental high-speed PCM system. Pairs of sequential bits are transposed to pairs of sequential ternary signals following specific rules such that any pair includes at least one positive or negative pulse. Preliminary tests of this code on a T1 carrier repeatered line have shown some degradation of line error rate due to the violation of the bipolar sequence. Further studies are required to determine whether this impairment may be offset by the benefits of the code.

5.2 *Error Rate*

A second general problem concerns T1 carrier system effects on data error rate. The correlation between line error rate and data error rate is dependent upon the data statistics, the terminal coding arrangement, and the distribution of line error rate between errors of omission and errors of commission.

For the series of terminals for asynchronous serial data, previously described, the data error rate may be from $\frac{1}{2}$ to 5 times the line error rate, depending upon the line error distribution. In the case of tape-to-computer data, the computer equipment provides for error checking. If one or more errors occur during transmission of a block of characters, the computer calls for retransmission of the block. In Fig. 21 the probability of a block retransmission, (P_R) is shown as a function of line error rate (P) for several block sizes, (R). It is apparent that line error rates poorer than 10^{-4} will result in little data "throughput" for

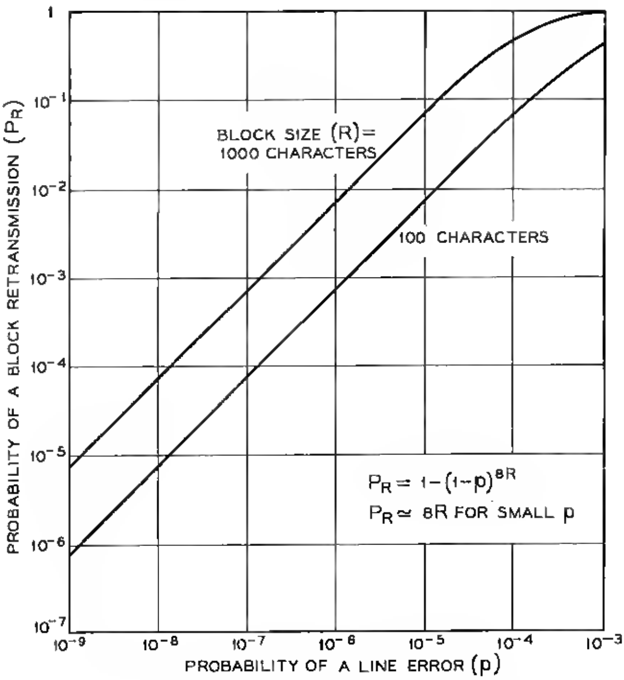


Fig. 21 — Probability of block retransmission.

block sizes of 1000 or more characters. By comparison, adequate, if somewhat degraded, voice frequency performance will result with D1 bank transmission at this error rate.

A study and test program is underway, the objective of which is to provide information on the statistics and distribution of line errors. Although the results are not conclusive, some preliminary tests have indicated that line error rates in the order of 10^{-8} may be expected for properly engineered and installed T1 carrier lines. To attain this capability, however, additional installation testing arrangements are required over those now employed for D1 bank signal transmission. For example, cases have occurred in which repeaters have been installed with incorrect line build-out networks, an error which was not discovered in the final testing procedures or by the terminal tests of the D1 bank. Under these conditions the line is extremely sensitive to line signal patterns which typically may be generated by the parallel data terminal. A simple test set generating such a pattern may provide one important test facility.

5.3 *Line Pattern Controls*

Associated with the error rate problem is the problem of data terminals producing certain fixed patterns on the line which may interfere with the timing of other systems. These patterns may be due to the data signal or due to the terminal coding process. This is of importance only in large cross-section systems on a single cable where lines carrying these interfering patterns make up a large part of this cross-section. Some control of pattern density may be obtained by selective code inversion of certain of the data signal bits in tbe transmitting terminal under the control of terminal timing. These would then be re-inverted in the receiving terminal. Such a change must be correlated, of course, with the control of the all-*ZERO* sequence.

VI. POTENTIAL TERMINAL APPLICATIONS

6.1 *Hybrid Terminal Arrangements*

The arrangements for multiplexing several like data signals has been described for the T1WB-1 and -2 wideband banks for serial data. These arrangements may be easily extended to include the multiplexing of different types of data signals wbich are processed into similar formats on the T1 carrier line. For example, a parallel data signal of the tape-to-computer type requiring only one-half the line capacity may be converted into alternate bits on the line. The remaining bit capacity may then be used for a combination of serial data signals requiring only one-half the line capacity. The timing circuits for this hybrid terminal arrangement may be common to both sets of equipment or separate timing circuits may be used if they are synchronized. It is clear, however, that data signals in this format on the line do not coordinate with the 8-bit word format of the D1 bank. Consider however, the conversion of the D1 bank signals into the format of the data signals. In Fig. 22, a D1 bank is shown, equipped with 12 channels in the even channel group. The output is transferred into a register which, under the control of timing, distributes tbe bits of the signal into alternate *EVEN* bits in the T1 carrier line. By synchronizing and framing the data timing circuits with this signal, the 12 voice channels may be interleaved with data signals occupying the *ODD* line bits. At the receiving end the *EVEN* bits are selected and transferred into a similar register where they are rearranged into the 8-bit word format.

An alternate arrangement for multiplexing voice and data signals may be obtained by converting the data signals into the D1 bank for-

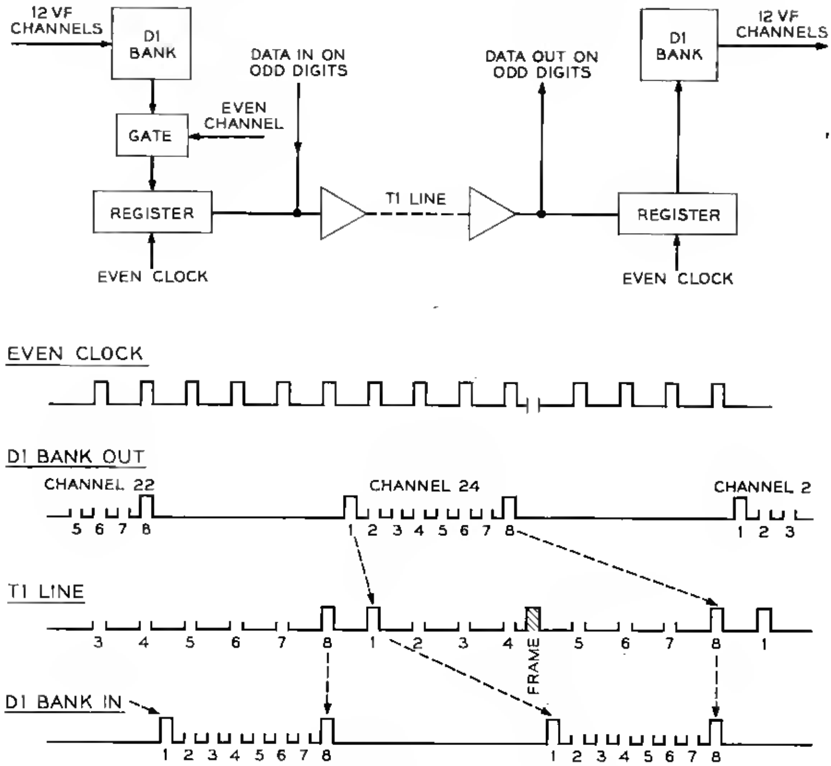


Fig. 22 — Multiplexing with a D1 Bank.

mat using similar register circuits in the reverse order to that described. Although the data would then appear in an 8-bit word group, and hence could be multiplexed with 12 channels from the D1 bank, it is not constrained in this format. That is, the organization of information in the data word bears no direct relationship with the channel word.

The advantage of one of these arrangements over the other is somewhat dependent upon the potential application. For the case where, say, three voice signals are to be replaced with one 50-kilobit serial data signal, it can be seen that less register storage capacity is required if the second alternative is applied. In this alternative the data signal is converted rather than the voice signals from the D1 bank. It is unlikely that a few voice signals from the D1 bank would be multiplexed with a majority of data signals. The cost of the D1 bank is such as to make it more attractive to transmit these few voice signals as part of a large group of voice signals over another T1 carrier line.

The first arrangement in which the data remains distributed bit-by-bit on the line, would appear to have one advantage, however. From the preliminary tests on line error distribution there is some evidence that a correlation in occurrence of errors exists such tbat there is a likelibood of errors occurring in adjacent or near adjacent time slots. By leaving multiplexed data in the distributed format, there is less likelihood of the event of paired errors occurring in only one channel, improving the effectiveness of simple error control coding which may exist in that channel signal.

6.2 *Synchronous Serial Data Terminals*

The terminals previously described for asynehronous serial data are, of course, capable of handling synchronous serial data at any rate up to a maximum rate determined by timing options. The penalty paid for this high degree of flexibility, however, is efficiency sinee tbree T1 carrier line bits are required for each data bit. The present eonditions in the data field as to the variety of data transmission requirements and the economics of T1 carrier relative to other facilities in the short-haul plant justify the use of this approach. However, if standard fixed rates for synchronous data transmission develop, terminals designed specifically for these fixed rates may be desirable. It is clear that for specific synchronous rates, efficiencies approaching one data bit per line bit are feasible.

The two approaches which are considered here do not require synchronization and phasing of the data source with the T1 carrier terminal clock. They do require, however, that the data be at specific rates within certain tolerance limits.

In the discussion of transmission of the parallel data terminal it was shown that large parallel characters can be put onto the T1 carrier line with fairly high efficiencies from tbe standpoint of T1 carrier bits required per data bit. This is due to the fact that only one timing or index bit is required to provide accurate timing for all of the bits of the character. This approach may be extended to synchronous serial data. Consider a synchronous serial data signal which is shifted in alternate groups of say 8 bits into 2 storage registers. These groups are transferred alternately into the parallel data terminal which transmits them on the T1 carrier line at a bit rate slightly higher than the original data bit rate. The average group rate on the line would be the same as the data group rate or $\frac{1}{8}$ the data bit rate. At the receiving end the data groups are transferred to a set of registers. The serial data is then read out of these registers under control of a "smoothing" clock

which derives its frequency control from the marking of the group rate or from a servo loop controlled by the status of storage in the registers.

One of the most promising approaches to efficient transmission of synchronous serial data signals involves the application of a technique proposed by J. S. Mayo for network synchronization of high-speed PCM systems.[6] Briefly, a synchronous serial bit stream of rate f_B may be processed into a line or fraction of a line with a capability f_L, slightly higher than f_B. By means of an elastic store and logic circuits, additional bits are "stuffed" into the bit stream f_B as necessary to make its rate identically f_L. Additional information is included on the line to identify the "stuffed" bits. At the receiving end the stuffed bits are removed, and the signal is smoothed in an elastic store. This technique will allow efficiencies approaching 100 per cent.

6.3 *T1 Carrier and High-Speed Digital Transmission Systems*

A plurality of wideband data signals, such as the 50-kilobit signal discussed earlier, can be transmitted over a T1 carrier repeatered line. In addition, the line has the capacity for considerably higher data rates, up to 1.5 megabits for synchronous serial signals.

T1 carrier was designed for application in the short haul plant. Presently, the signals transmitted via a T1 carrier end link must be brought down to baseband and transformed by analog terminals for long haul transmission. One may expect that digital transmission techniques will be adopted in the toll plant in the future, thus providing a broader use for a variety of digital data terminals such as those considered in this article.

VII. ACKNOWLEDGMENTS

The work described in this article is the result of the efforts of many in the engineering and development organizations of Bell Laboratories. The writers particularly wish to acknowledge the contributions of Messrs. R. G. DeWitt and J. P. Forde, whose planning and evaluation of the experimental service among the Bell Laboratories computation centers provided important data for the development program.

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